MC33178, MC33179

Low Power, Low Noise Operational Amplifiers

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 μA of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open−loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions in several package options.

Features

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.0024% (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/μs
- Dual Supply Operation: ±2.0 V to ±18 V
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance
- Pb−Free Packages are Available

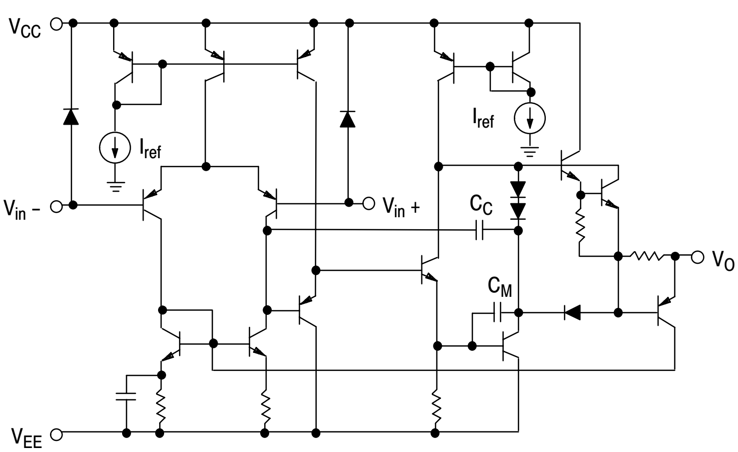
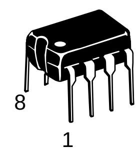


Figure 1. Representative Schematic Diagram
(Each Amplifier)

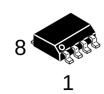
ON Semiconductor®

http://onsemi.com

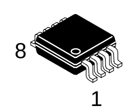
DUAL



PDIP−8
P SUFFIX
CASE 626

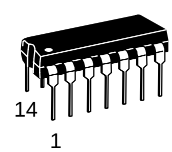


SOIC−8
D SUFFIX
CASE 751

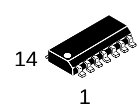


Micro8
DM SUFFIX
CASE 846A

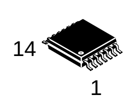
QUAD



PDIP−14
P SUFFIX
CASE 646



SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 4 of this data sheet.

October, 2005 − Rev. 6
Publication Order Number:
MC33178/D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	Note 2	mW
Operating Temperature Range	T_A	−40 to +85	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 2.)

ORDERING INFORMATION

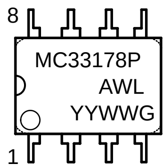
Device	Package	Shipping†
MC33178D	SOIC−8	98 Units / Rail
MC33178DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33178DR2	SOIC−8	2500 / Tape & Reel
MC33178DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC33178P	PDIP−8	1000 Units / Rail
MC33178PG	PDIP−8 (Pb−Free)	1000 Units / Rail
MC33178DMR2	Micro8	4000 / Tape & Reel
MC33178DMR2G	Micro8 (Pb−Free)	4000 / Tape & Reel
MC33179D	SOIC−14	55 Units / Rail
MC33179DG	SOIC−14 (Pb−Free)	55 Units / Rail
MC33179DR2	SOIC−14	2500 / Tape & Reel
MC33179DR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC33179P	PDIP−14	500 Units / Rail
MC33179PG	PDIP−14 (Pb−Free)	500 Units / Rail
MC33179DTBR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

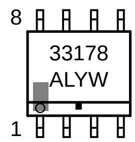
MARKING DIAGRAMS

DUAL

PDIP−8
CASE 626

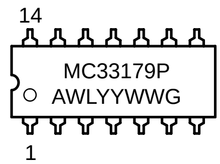


SOIC−8
CASE 751

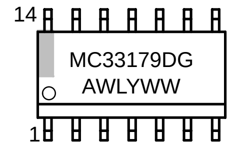


QUAD

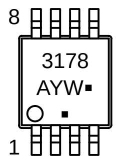
PDIP−14
CASE 646



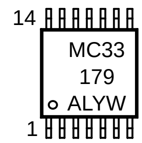
SOIC−14
CASE 751A



Micro8
CASE 846A



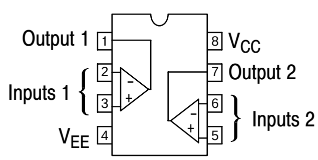
TSSOP−14
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G, ▪ = Pb−Free Package
(Note: Microdot may be in either location)

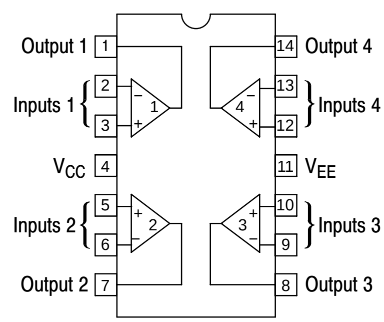
PIN CONNECTIONS

DUAL
CASE 626/751/846A



(Top View)

QUAD
CASE 646/751A/948G



(Top View)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\|V_{IO}\|$				mV
(V_{CC} = +2.5 V, V_{EE} = −2.5 V to V_{CC} = +15 V, V_{EE} = −15 V)						
T_A = +25°C			−	0.15	3.0	
T_A = −40° to +85°C			−	−	4.0	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\Delta V_{IO}/\Delta T$				μV/°C
T_A = −40° to +85°C			−	2.0	−	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			−	100	500	
T_A = −40° to +85°C			−	−	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			−	5.0	50	
T_A = −40° to +85°C			−	−	60	
Common Mode Input Voltage Range	6	V_{ICR}	−13	−14	−	V
(ΔV_{IO} = 5.0 mV, V_O = 0 V)			−	+14	+13	
Large Signal Voltage Gain (V_O = −10 V to +10 V, R_L = 600 Ω)	7, 8	A_{VOL}				kV/V
T_A = +25°C			50	200	−	
T_A = −40° to +85°C			25	−	−	
Output Voltage Swing (V_{ID} = ±1.0 V)	9, 10, 11					V
(V_{CC} = +15 V, V_{EE} = −15 V)						
R_L = 300 Ω		V_O+	−	+12	−	
R_L = 300 Ω		V_O-	−	−12	−	
R_L = 600 Ω		V_O+	+12	+13.6	−	
R_L = 600 Ω		V_O-	−	−13	−12	
R_L = 2.0 kΩ		V_O+	+13	+14	−	
R_L = 2.0 kΩ		V_O-	−	−13.8	−13	
(V_{CC} = +2.5 V, V_{EE} = −2.5 V)						
R_L = 600 Ω		V_O+	1.1	1.6	−	
R_L = 600 Ω		V_O-	−	−1.6	−1.1	
Common Mode Rejection (V_{in} = ±13 V)	12	CMR	80	110	−	dB
Power Supply Rejection	13	PSR				dB
V_{CC}/V_{EE} = +15 V/ −15 V, +5.0 V/ −15 V, +15 V/ −5.0 V			80	110	−	
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground)	14, 15	I_{SC}				mA
Source (V_{CC} = 2.5 V to 15 V)			+50	+80	−	
Sink (V_{EE} = −2.5 V to −15 V)			−50	−100	−	
Power Supply Current (V_O = 0 V)	16	I_D				mA
(V_{CC} = 2.5 V, V_{EE} = −2.5 V to V_{CC} = +15 V, V_{EE} = −15 V)						
MC33178 (Dual)						
T_A = +25°C			−	−	1.4	
T_A = −40° to +85°C			−	−	1.6	
MC33179 (Quad)						
T_A = +25°C			−	1.7	2.4	
T_A = −40° to +85°C			−	−	2.6	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	17, 32	SR	1.2	2.0	−	V/μs
Gain Bandwidth Product (f = 100 kHz)	18	GBW	2.5	5.0	−	MHz
AC Voltage Gain (R_L = 600 Ω, V_O = 0 V, f = 20 kHz)	19, 20	A_{VO}	−	50	−	dB
Unity Gain Bandwidth (Open−Loop) (R_L = 600 Ω, C_L = 0 pF)		BW	−	3.0	−	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	21, 23, 24	A_m	−	15	−	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	22, 23, 24	ϕ_m	−	60	−	Deg
Channel Separation (f = 100 Hz to 20 kHz)	25	CS	−	−120	−	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 600 Ω, THD ≤ 1.0%)		BW_p	−	32	−	kHz
Total Harmonic Distortion (R_L = 600 Ω,, V_O = 2.0 V_{pp}, A_V = +1.0 V)	26	THD				%
(f = 1.0 kHz)			−	0.0024	−	
(f = 10 kHz)			−	0.014	−	
(f = 20 kHz)			−	0.024	−	
Open Loop Output Impedance (V_O = 0 V, f = 3.0 MHz, A_V = 10 V)	27	$\lvert Z_O \rvert$	−	150	−	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	−	200	−	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	−	10	−	pF
Equivalent Input Noise Voltage (R_S = 100 Ω,)	28	e_n				nV/√Hz
f = 10 Hz			−	8.0	−	
f = 1.0 kHz			−	7.5	−	
Equivalent Input Noise Current	29	i_n				pA/√Hz
f = 10 Hz			−	0.33	−	
f = 1.0 kHz			−	0.15	−	

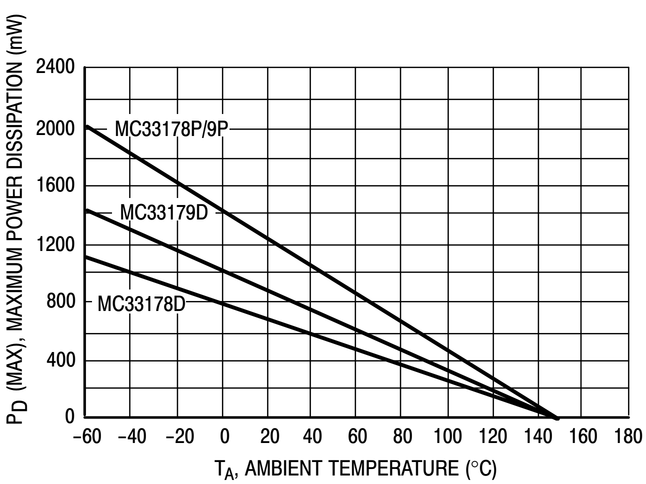


Figure 2. Maximum Power Dissipation versus Temperature

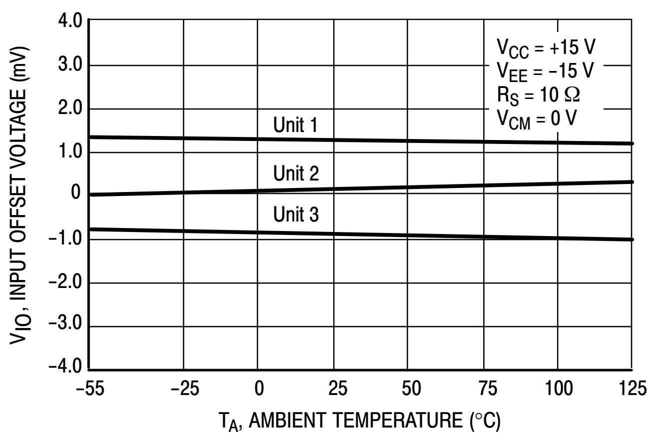


Figure 3. Input Offset Voltage versus Temperature for 3 Typical Units

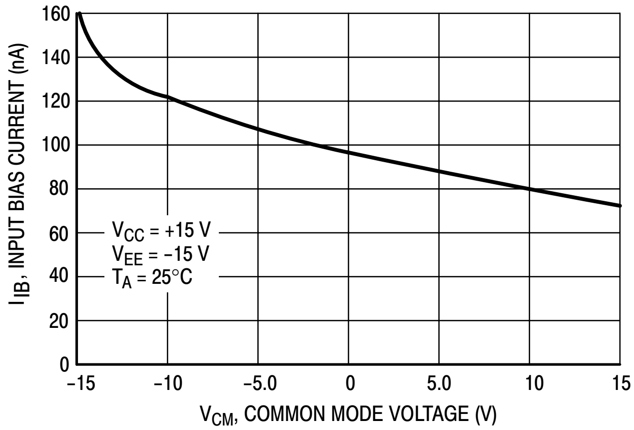


Figure 4. Input Bias Current versus Common Mode Voltage

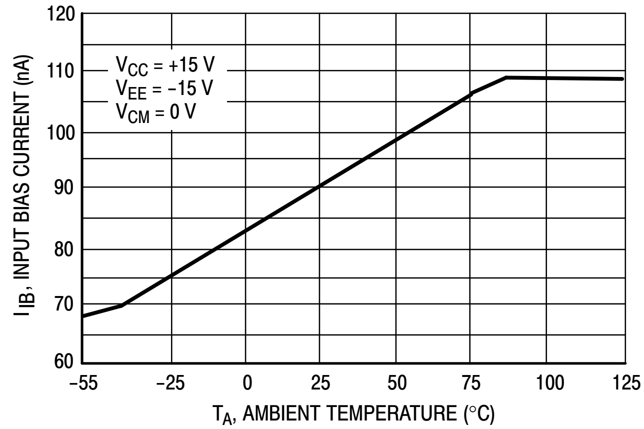


Figure 5. Input Bias Current versus Temperature

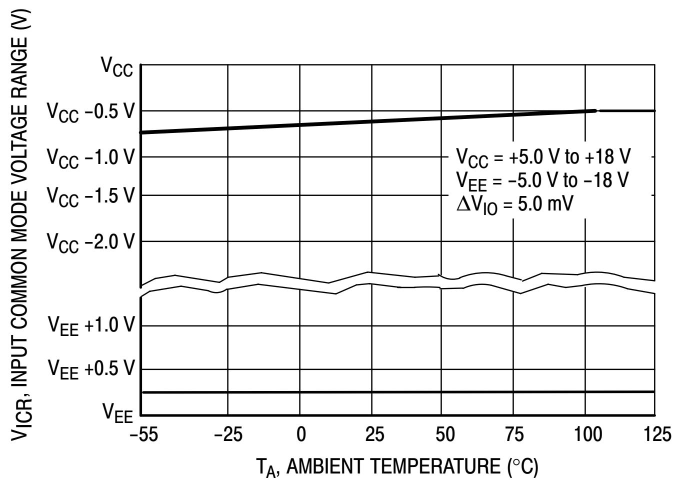


Figure 6. Input Common Mode Voltage Range versus Temperature

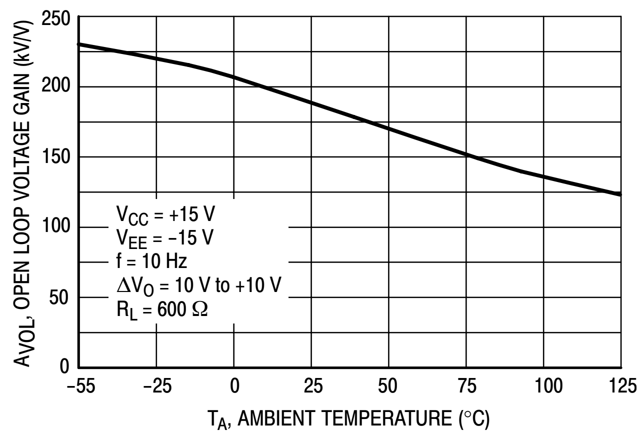


Figure 7. Open Loop Voltage Gain versus Temperature

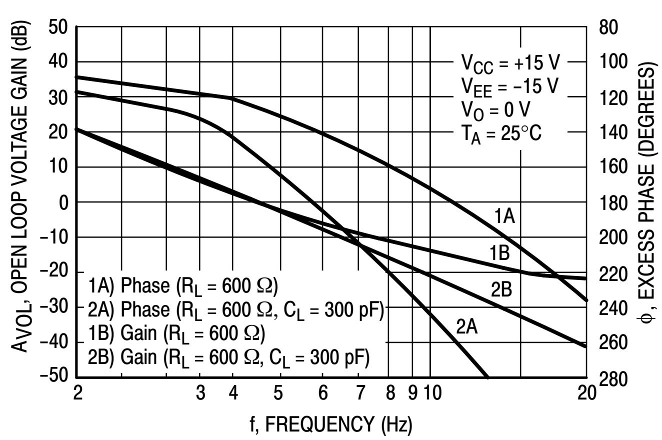


Figure 8. Voltage Gain and Phase versus Frequency

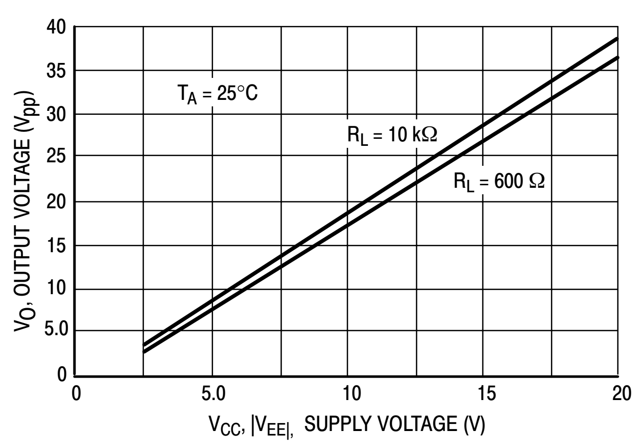


Figure 9. Output Voltage Swing versus Supply Voltage

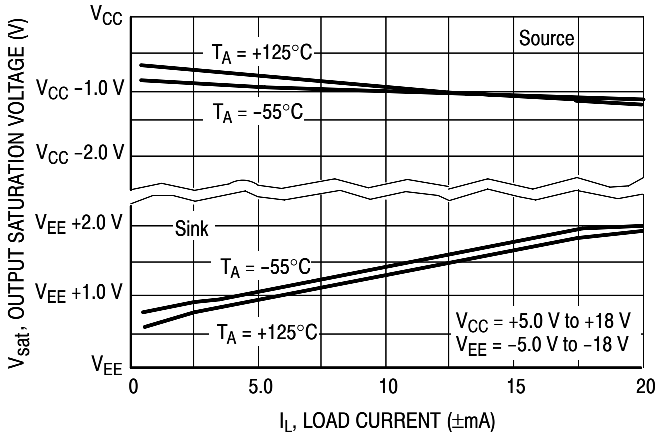


Figure 10. Output Saturation Voltage versus Load Current

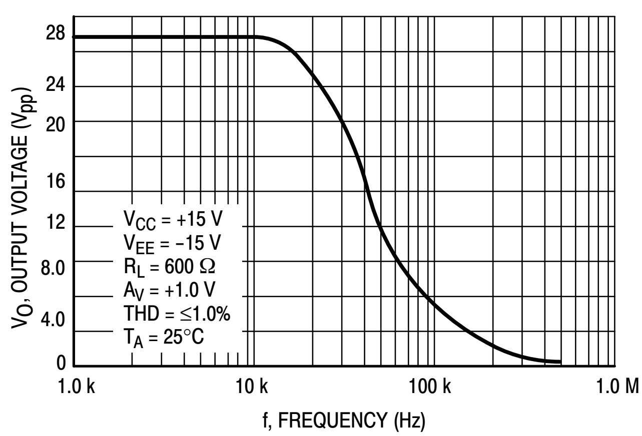


Figure 11. Output Voltage versus Frequency

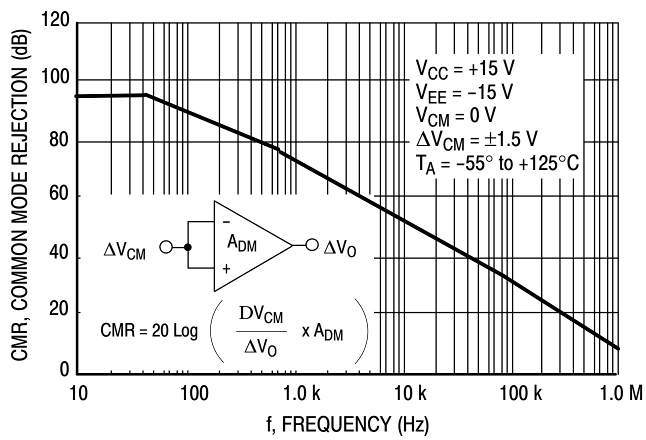


Figure 12. Common Mode Rejection versus Frequency Over Temperature

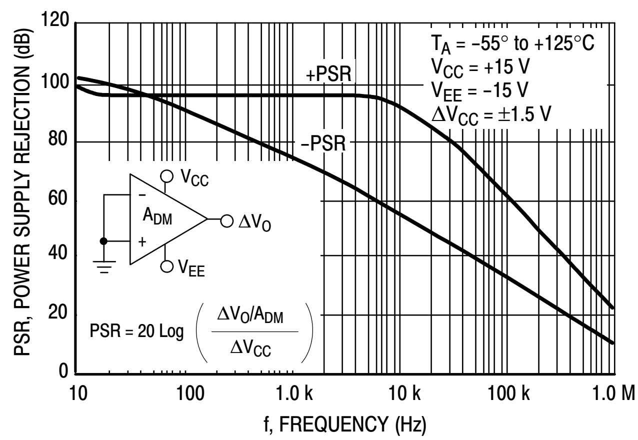


Figure 13. Power Supply Rejection versus Frequency Over Temperature

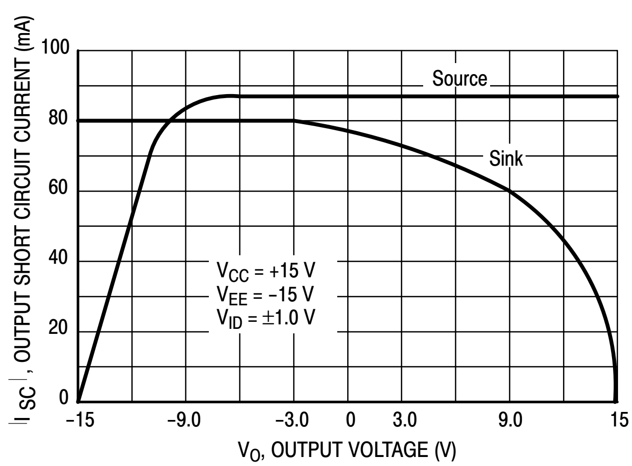


Figure 14. Output Short Circuit Current versus Output Voltage

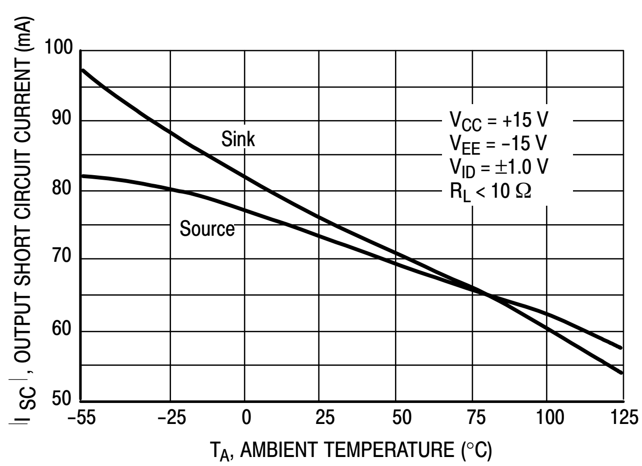


Figure 15. Output Short Circuit Current versus Temperature

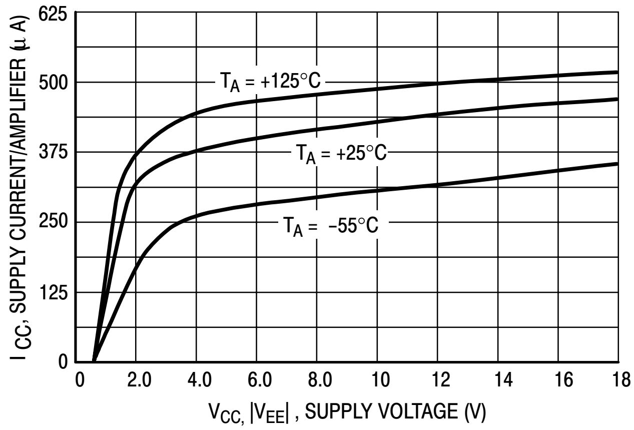


Figure 16. Supply Current versus Supply Voltage with No Load

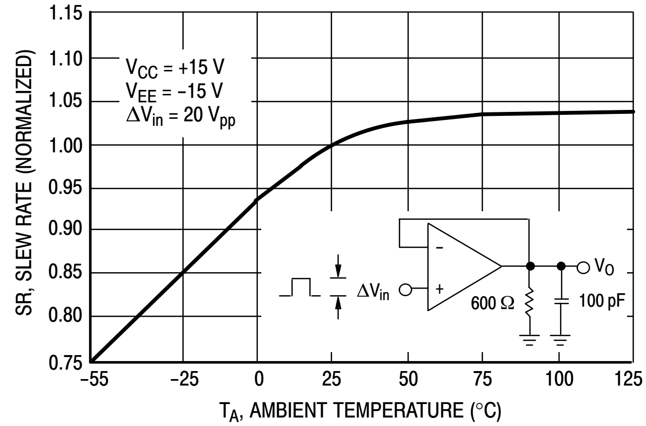


Figure 17. Normalized Slew Rate versus Temperature

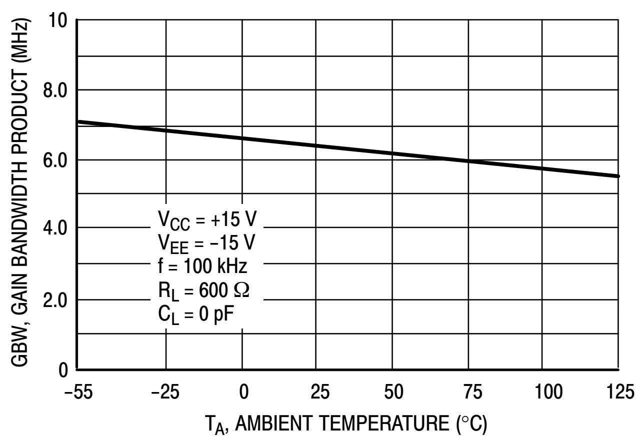


Figure 18. Gain Bandwidth Product versus Temperature

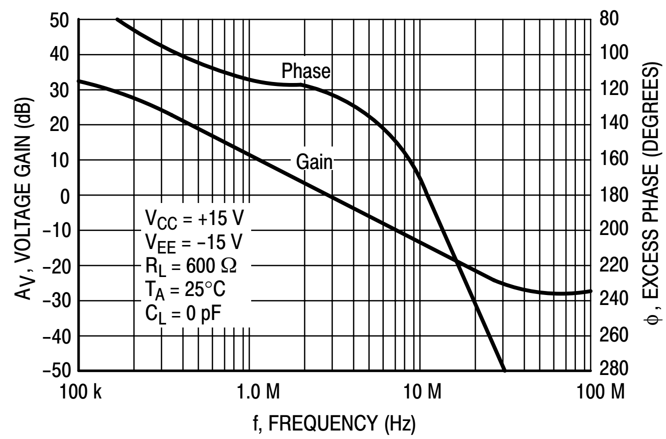


Figure 19. Voltage Gain and Phase versus Frequency

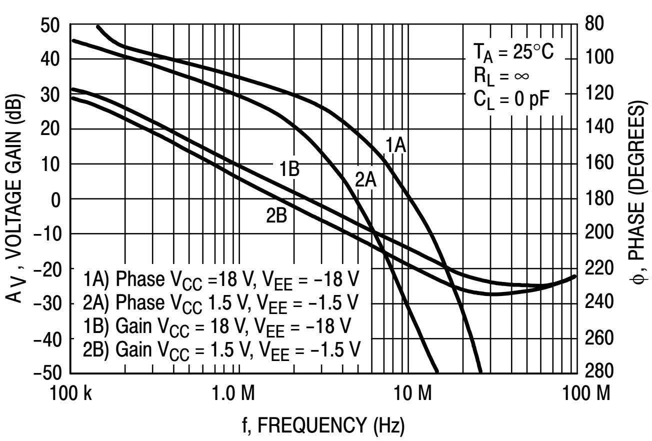


Figure 20. Voltage Gain and Phase versus Frequency

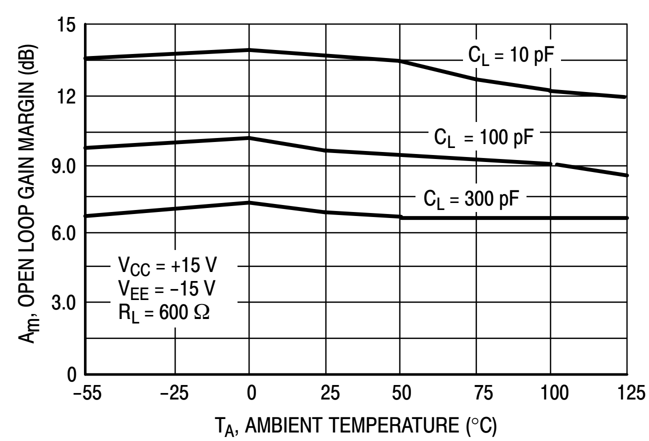


Figure 21. Open Loop Gain Margin versus Temperature

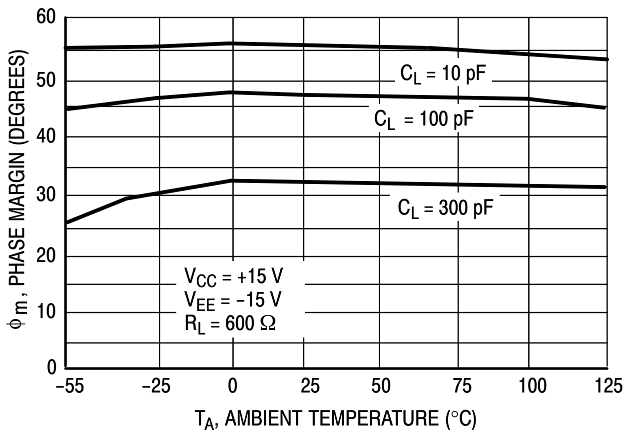


Figure 22. Phase Margin versus Temperature

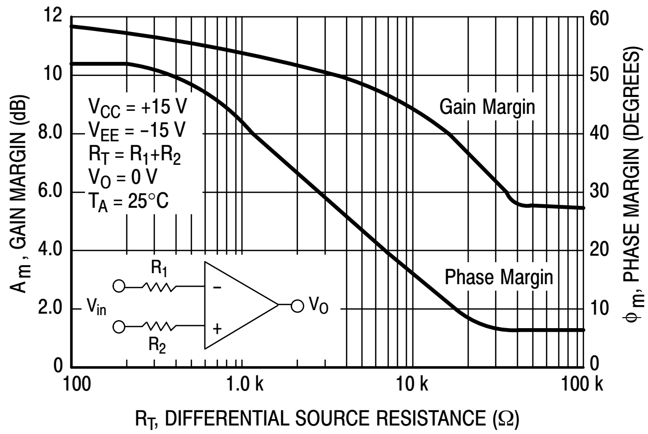


Figure 23. Phase Margin and Gain Margin versus Differential Source Resistance

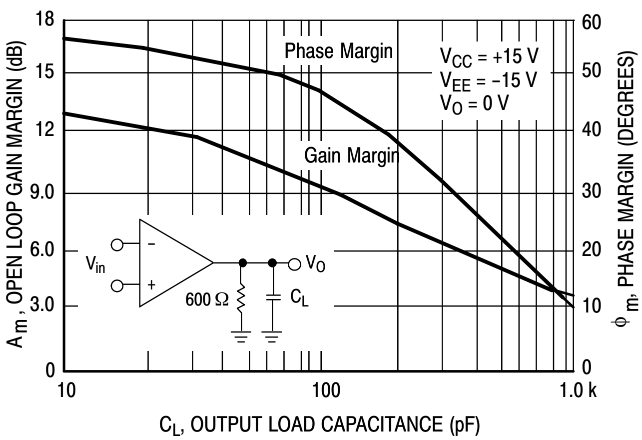


Figure 24. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

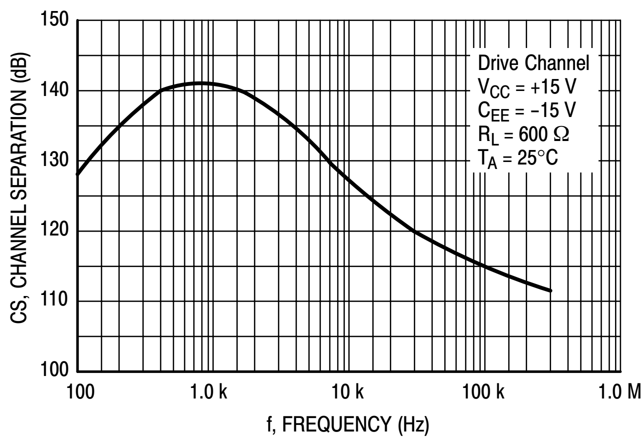


Figure 25. Channel Separation versus Frequency

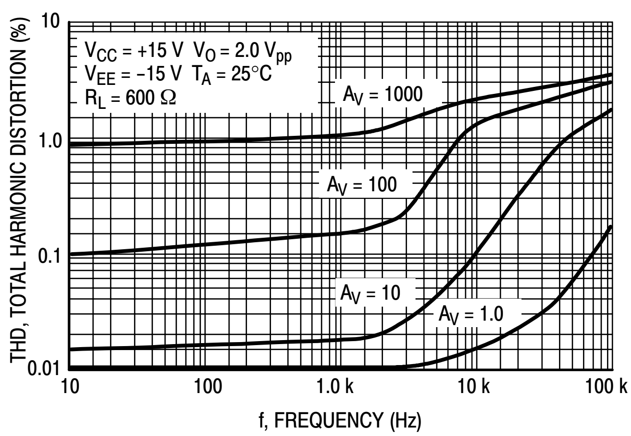


Figure 26. Total Harmonic Distortion versus Frequency

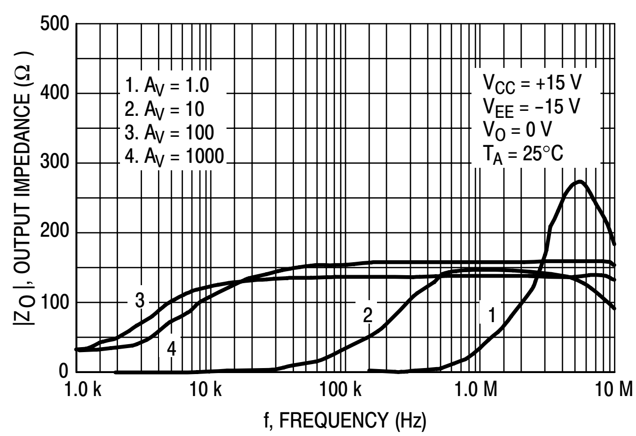


Figure 27. Output Impedance versus Frequency

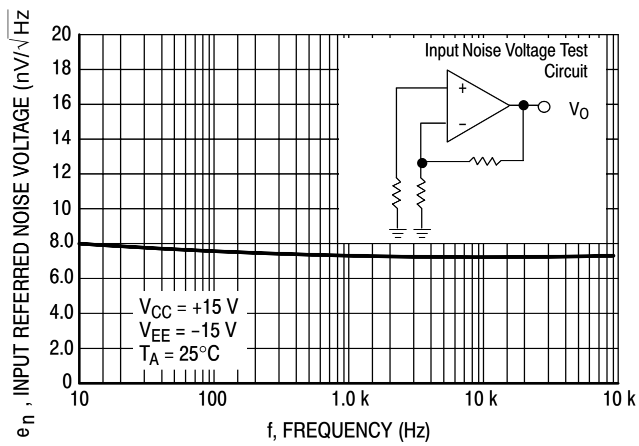


Figure 28. Input Referred Noise Voltage versus Frequency

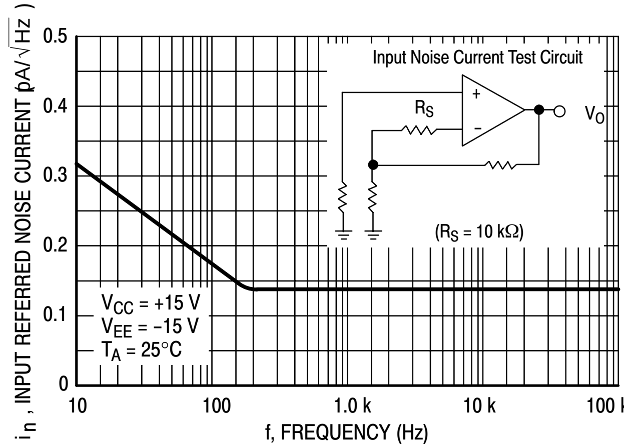


Figure 29. Input Referred Noise Current versus Frequency

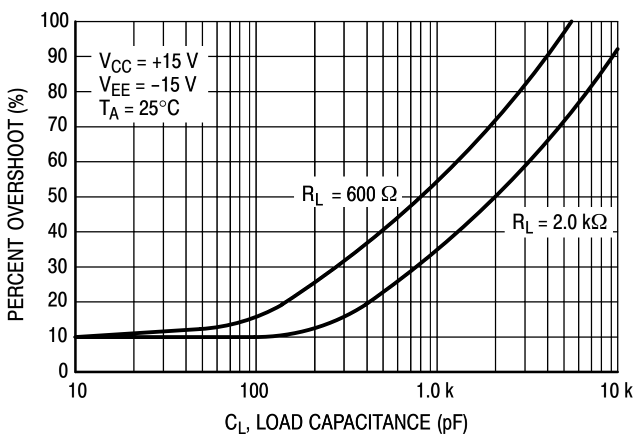


Figure 30. Percent Overshoot versus Load Capacitance

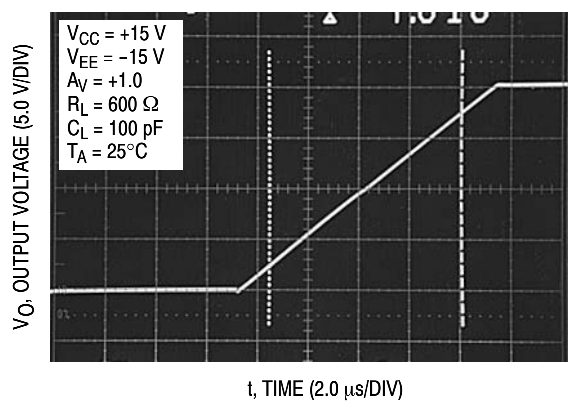


Figure 31. Non−inverting Amplifier Slew Rate

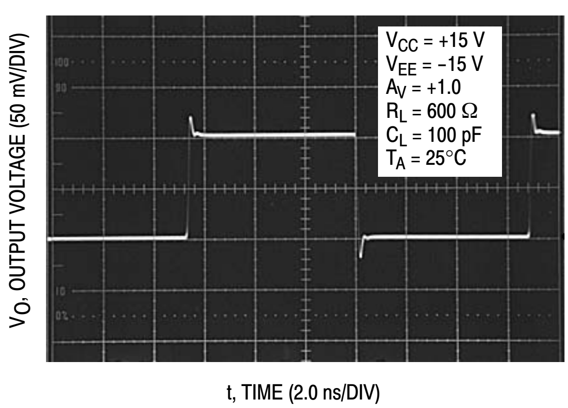


Figure 32. Small Signal Transient Response

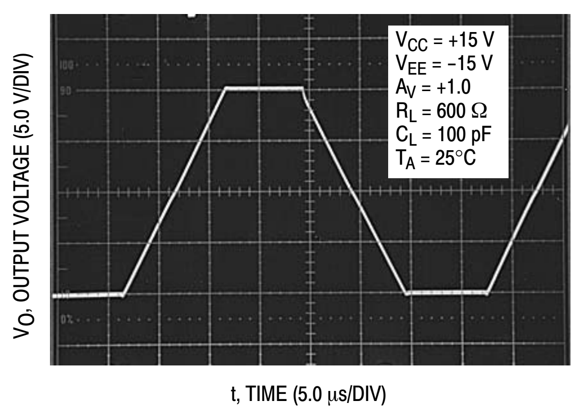


Figure 33. Large Signal Transient Response

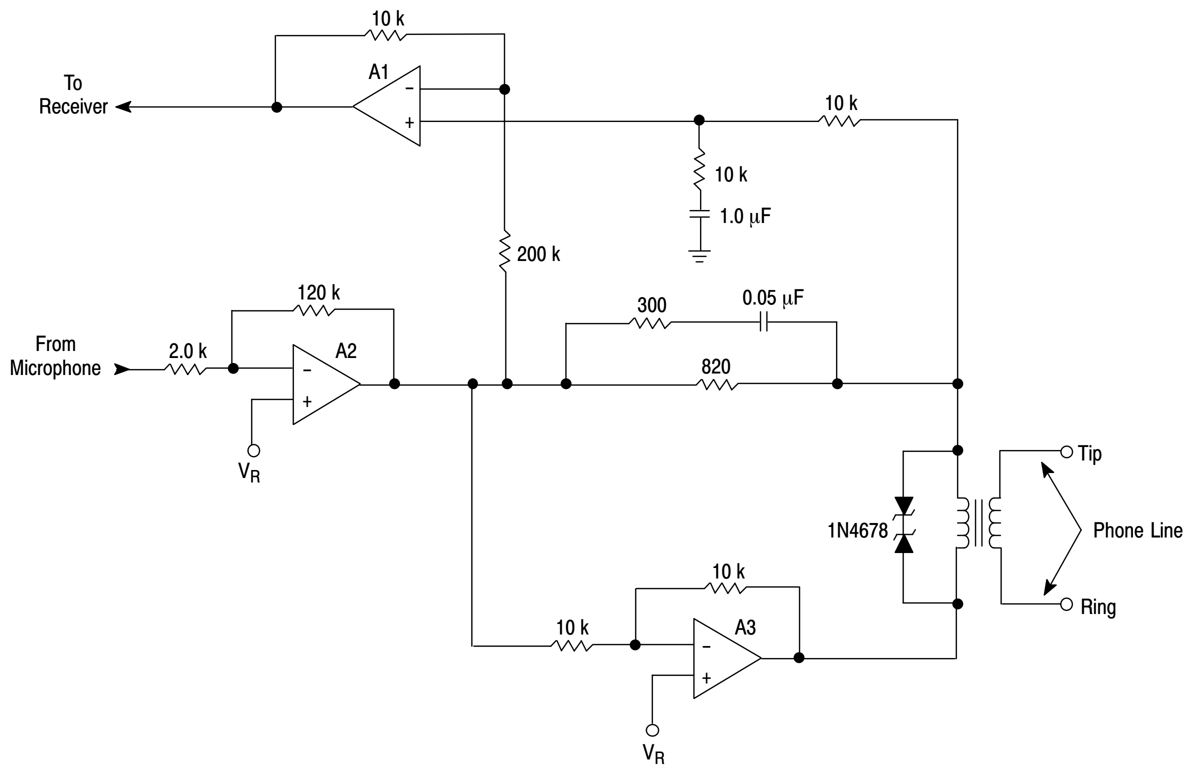


Figure 34. Telephone Line Interface Circuit

APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 24). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 34 both A2 and A3 are driving equivalent loads of approximately 600 Ω.

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion, is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous “pick up” at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used (R1 > 1.0 kΩ), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 35) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance, it is important to choose the optimum value for that capacitor. This can be determined by the following Equation:

$$C_C = (1 + [R1/R2])^2 \times C_L (Z_O/R_2) \quad (1)$$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads (500 pF < C_L < 1500 pF) the addition of a compensation resistor on the order of 20 Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 36). For high capacitive loads (C_L > 1500 pF), a combined compensation scheme should be used (see Figure 37). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using Equation 1. The Equation to calculate R_C is as follows:

$$R_C = Z_O \times R1/R2 \quad (2)$$

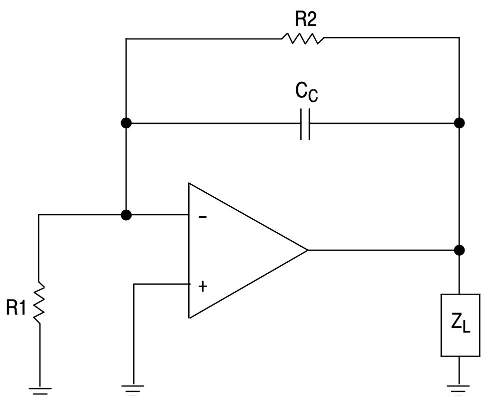


Figure 35. Compensation for High Source Impedance

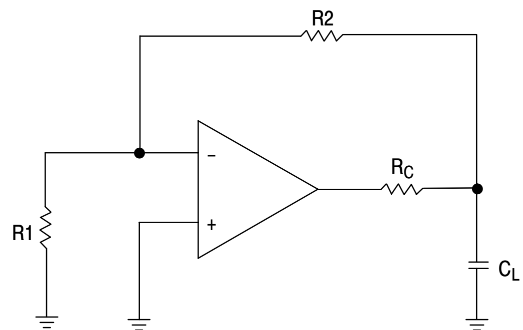


Figure 36. Compensation Circuit for Moderate Capacitive Loads

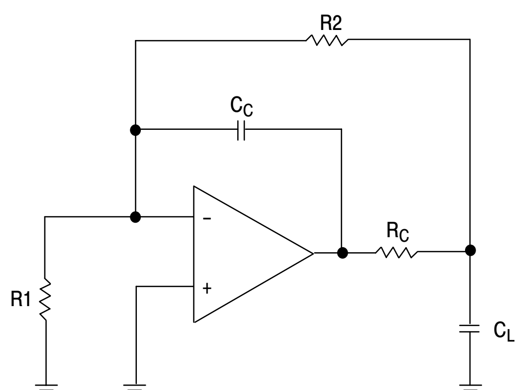
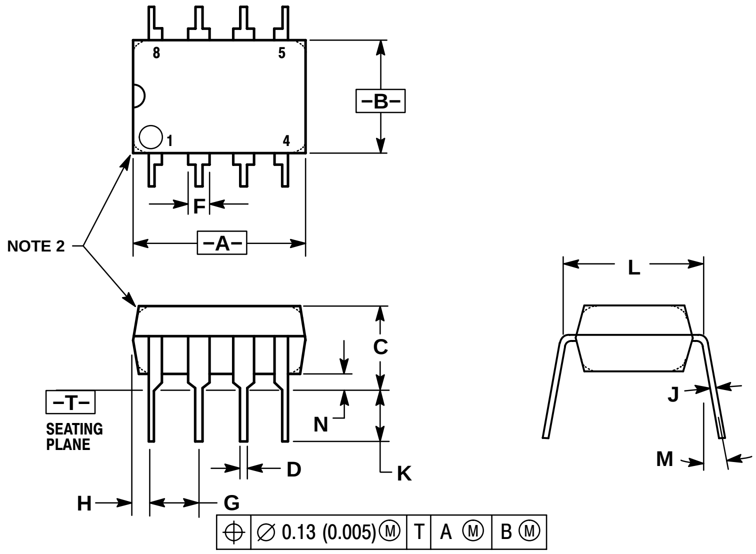


Figure 37. Compensation Circuit for High Capacitive Loads

PACKAGE DIMENSIONS

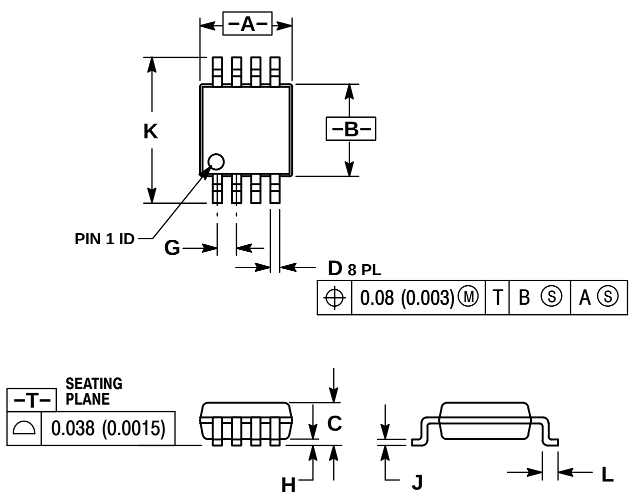
PDIP−8
P SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

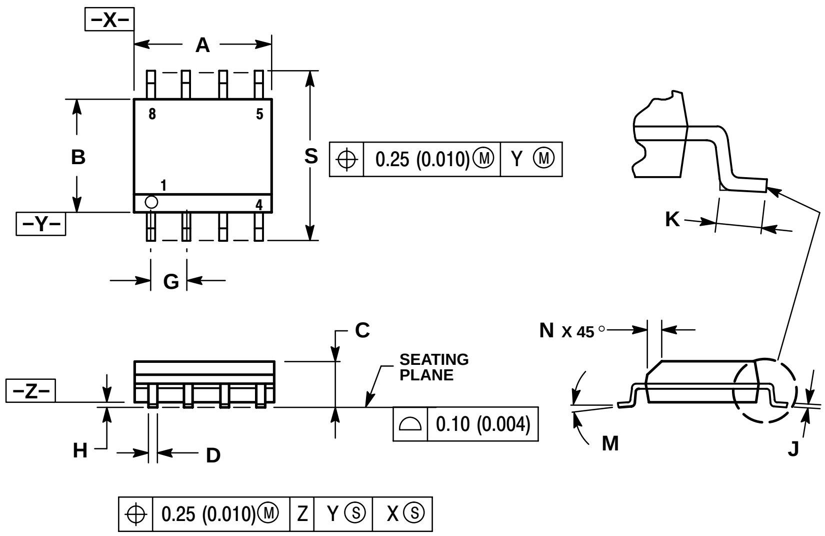
Micro8
DM SUFFIX
CASE 846A−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

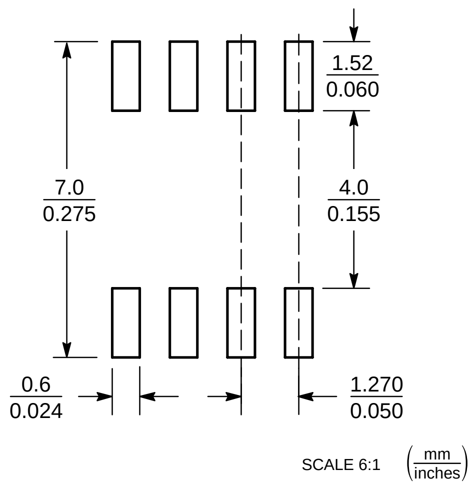
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

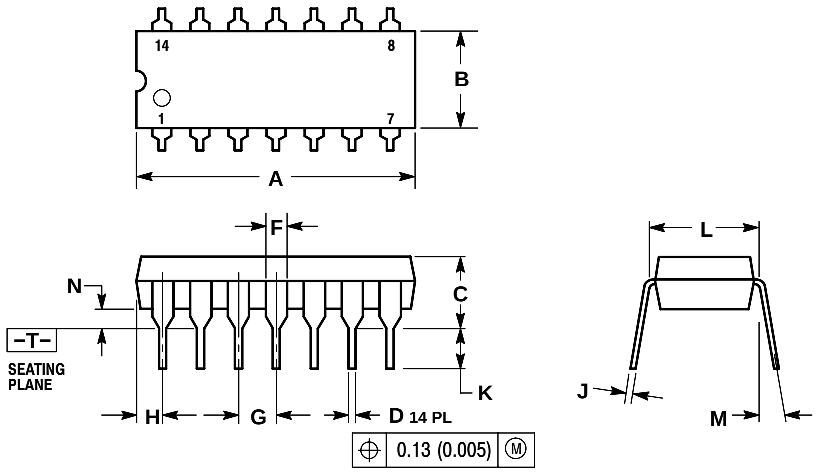
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

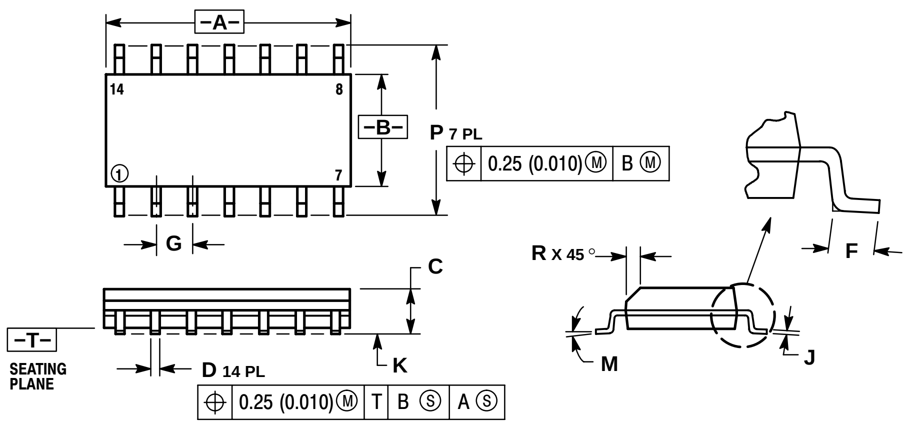
PDIP−14
P SUFFIX
CASE 646−06
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SOIC−14
D SUFFIX
CASE 751A−03
ISSUE G

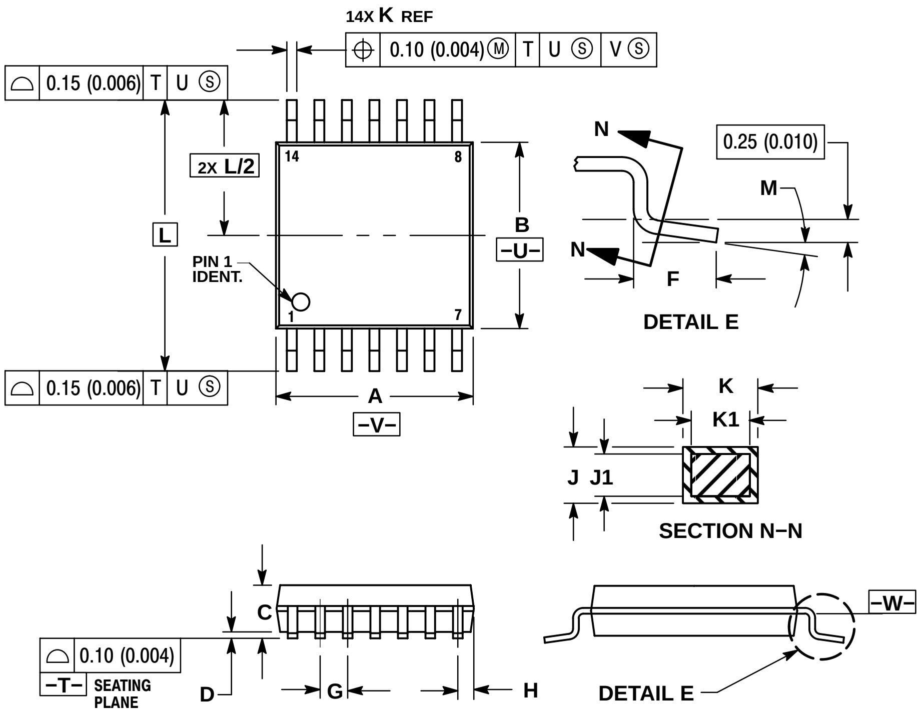


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP−14
DTB SUFFIX
CASE 948G−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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